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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/673,137 | 09/30/2003 | Shigeto Kobayashi | 65933-048 | 3822 |

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| EXAMINER | |
|---|---|
| MAI, LAM T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/673,137 | KOBAYASHI, SHIGETO | |
| | Examiner | Art Unit | |
| | LAM T MAI | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3* is/are allowed.

6)☒ Claim(s) *4,5,8,11,14 and 15* is/are rejected.

7)☒ Claim(s) *6,7,9,10,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/7/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

2. The information disclosure statement (IDS) submitted on 1/7/2004, has been considered by the examiner.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 4-5, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Nikai et al (USP 6,683,554).

4. Regarding claim 4, Nikai discloses a pipeline analog to digital conversion ciruit in figures 1-3 that teaches:

a first adjustment unit that set a level of a reference signal according to a range of an input signal so that values of the input signal fall within a satisfactory range in terms of conversion performance thereof (figures 2,3; element (90); col. 24, lines 39-65), and

a second adjustment unit that set a offset (figure 1, element 12) temporary variation which is caused in the input signal and by operation of the reference signal, during converting the input signal into a target signal (figures 2,3; element (90); col. 24, lines 39-65).

5. Regarding claim 5, Nikai discloses a pipeline analog to digital conversion circuit in figures 1-3 that teaches:

a first adjustment unit that set level of a reference signal is set according to a range of an input signal so that values of the input signal fall within a satisfactory range in terms of conversion performance thereof (figures 2,3; element (90); col. 24, lines 39-65),

an analog to digital conversion unit (Dn – D1, in figure 2), which convert the value of the input analog voltage into digital values; and

a second adjustment unit that set a offset (figure 1, element 12) temporary variation which is caused in the value of the input analog voltage and as a result of the reference signal operated during a-d conversion (figures 2,3; element (90); col. 24, lines 39-65).

6. Regarding claim 8, Nikai discloses a pipeline analog to digital conversion circuit in figure 1, that also teaches plural stages of conversion units (elem. 3,4,5,6) at each of which one or more bit digital values are generated gradually staring from a high-order bit (first stage (3) generated 4 bits; second stage (4) generated 2 bits; third stage (5) generated 2 bits and fourth stage (6) generated 2 bits) and any of the plural stages of conversion units includes or include first adjust unit (9) and second adjustment unit (12).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11, and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by McCarroll USP 6,211,806.

7. Regarding claim 11, McCarroll disclose in figure 1 a pipeline analog to digital converter that teaches:

a analog to digital conversion units (10,20,30,40) which acquire an input analog voltage value and the converts the acquired input analog voltage value into a digtal value of a predetermined bit number; and

a sample and hold units (15,25,35,45) which acquire and hold a value adjusted so that input analog voltage to be acquired by the a-d conversion unit falls within a satisfactory range in terms of conversion performance thereof (see col. 2 and 3).

8. Regarding claim 14, McCarroll teaches in figure 1 that the input analog value is inputted, as it is, to analog to digital converter (11) and an adjusted value of the input analog value is inputted to a sample and hold circuit (15).

9. Regarding claim 15, McCarroll teaches in figure 1 that the value to be inputted to the sample and hold (25) is a value obtained by again converting output from the a-d converter (11) into analog value (12) and subtracting (16) converted analog value from the input analog value (AIN).

***Allowable Subject Matter***

10. Claims 1-3 are allowable. Claims 1-3 are allowed over the prior art of record. The prior art fails to teach or suggest a method for converting a signal that teaches holding a signal value obtained as a result of adjustment to the input signal value using

the reference signal and converting the input signal to a target signal in parallel with the holding.

11. Claims 6-7, 9-10, and 13 are objected to as being dependent upon a rejected base claim 5, but they would be considered for allowance if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 6-7, 9-10 and 13 appear containing allowable subject mater because the prior art of record fails to teach or suggest the first adjustment unit includes a comparator for determining the range of the input analog voltage, and a sample and hold unit which holds a value obtained in a manner such that temporary variation is added to the value of the input analog voltage based on the thus set reference signal so that the values of the input analog voltage fall within the satisfactory range.

12. Claim 12 is objected to as being dependent upon a rejected base claim 4, but it would be considered for allowance if they are rewritten in independent form including all of the limitation of the base claim and any intervening claims. Claims 13 appear to be allowable because the prior art of record fails to teach or suggest a teach of adding artificial variation to input voltage which may cause error to output of a sample and hold circuit, on the condition that the added artificial variation is offset at a later stage.

**Cite References**

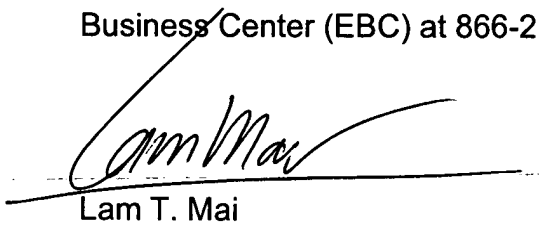
13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S Patents 6,6,83,554; 6,304,206; 6,211,806; 6,456,211 disclose pipeline analog to digital converter with increased conversion speed and high conversion accuracy.

***Conclusion***

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM T MAI whose telephone number is (571)272-1807. The examiner can normally be reached on 6:00 am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lam T. Mai
Art Unit 2819